UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/843,486	04/25/2001	Arash Hassibi	004363.P004	9275

7590 08/07/2002

Edwin H. Taylor
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	3

DATE MAILED: 08/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/843,486	HASSIBI ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claim 10 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim 9. See MPEP § 608.01(n). Accordingly, the claim10 has not been further treated on the merits.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,209,119 to Fukui.

Regarding claim 1, Fukui teaches a method for designing a circuit where design parameters for performance specifications are represented by posynomial expressions with constraints and solved with geometric programming, an improvement for simultaneously determining the boundaries for circuit elements in the floor plan of the circuit comprising:

representing the boundaries for circuit elements in the floor plan of the circuit as posynomial expressions with constraints on circuit size;

solving the posynomial expressions for the design parameters and floor plan boundaries on a digital computer using geometric programming;

outputting the results in a format that can be used by a circuit designer in the fabrication of the circuit (see figures 1-16).

Regarding claim 2, Fukui teaches the representation of the floor plan of the circuit includes the slicing of the circuit along the boundaries of the circuit elements (column 12, lines 21-24, 53-55; column 13, lines 6-8).

Regarding claim 3, Fukui teaches using layout constraints for the floor plan (see figures 5, 14; column 3, lines 1-5; column 7, lines 5-15).

Regarding claim 4, Fukui teaches one layout constraint is a limitation on the circuit area (see figures 1, 5; column 7, lines 5-15).

Regarding claim 5, Fukui teaches that another layout constraint is a limitation on the aspect ratio of the circuit layout (see figures 10 and 11; column 8, lines 36 – 67).

Regarding claim 6, Fukui teaches a method for designing an analog integrated circuit having active circuit elements where design parameters for performance specifications are represented by posynomial expressions with constraints and then solved with geometric programming, an improvement for simultaneously determining the boundaries for the active circuit elements in a floor plan for the integrated circuit comprising:

representing the floor plan as posynomial constraints of vertical and horizontal dimensions for each of the active circuit elements;

solving the posynomial expressions for the design parameters and vertical and horizontal dimensions; and

outputting the results of the preceding step in a format usable for a circuit designer to fabricate the integrated circuit (see figures 1-16).

Regarding claim 7, Fukui teaches the integrated circuit is sliced vertically and horizontally along the boundaries of the circuit elements (see figure 16 a-c; column 12, line 57 – column 13, line 2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,209,119 to Fukui.

Regarding claim 8, Fukui teaches vertically and horizontally sliced nodes (see figures 16 a-c; column 12, line 50 – column 13, line 11). Fukui does not teach the resulting first sibling nodes are represented by a sum of horizontal dimensions of the first sibling nodes being equal to or less than a first parent node and which dimensions of the first sibling nodes each being equal to or less than a vertical dimension of the first parent node. It would have been obvious to one having ordinary skill in the art at the time the invention was made to represent a sum of horizontal dimensions of the first sibling nodes being equal to or less than a first parent node and which dimensions of the first sibling nodes each being equal to or less than a vertical dimension of the first parent node for the intended use.

Regarding claim 9, Fukui teaches vertically and horizontally sliced nodes (see figures 6 a-c; column 12, line 50 – column 13, line 11). Fukui does not teach the resulting second sibling nodes are represented by the sum of the vertical dimensions of the second sibling nodes being equal to or less than a second parent node, and the horizontal dimensions of second sibling nodes each being equal to or less than a vertical height of the second parent node. It would have been obvious to one having ordinary skill in the art at the time the invention was made to represent the sum of the vertical dimensions of the second sibling nodes being equal to or less than a second parent node, and the horizontal dimensions of second sibling nodes each being equal to or less than a vertical height of the second parent node for the intended use.

Regarding claim 10, Fukui teaches the circuit elements include MOS transistor where the vertical dimension and horizontal dimension of each of the MOS transistors is represented by a posynomial expression (column 8, lines 2-6).

Regarding claim 11, Fukui teaches the posynomial expression for the vertical and horizontal dimensions of the MOS transistors include process dependant parameters (see figures 6 and 16 a-c; column 7, lines 19-30; column 13, lines 24-25).

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,209,119 to Fukui in view of US Patent No. 6,269,277 to Hershenson et al.

Regarding claim 12, Fukui does not teach the design of the analog circuit presupposes that the active circuit elements are operating in their saturation regions. However, Hershenson et al. teach the design of the analog circuit presupposes that the active circuit elements are operating in their saturation regions (column 11, line 11; column 13, line 6 – column 14, line 2). Therefore, it

would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hershenson et al. into the method taught by Fukui, since the transistors remain in saturation for all possible values of the input common-mode voltage and the output voltage and the constraints are each posynomial inequalities of the design variables and hence can be handled by geometric programming.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tom Thomas

QVU
August 5, 2002

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800